A Step-up Resonant Converter for Grid-Connected Renewable Energy Sources

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***Abstract*—With the rapid development of large-scale renewable energy sources and HVDC grid, it is a promising option to connect the renewable energy sources to the HVDC grid with a pure dc system, in which high-power high-voltage step-up dc–dc converters are the key equipment to transmit the electrical energy. This paper proposes a resonant converter which is suitable for grid-connected renewable energy sources. The converter can achieve high voltage gain using an *LC* parallel resonant tank. It is characterized by zero-voltage-switching (ZVS) turn-on and nearly ZVS turn-off of main switches as well as zero-current-switching turn-off of rectifier diodes; moreover, the equivalent voltage stress of the semiconductor devices is lower than other resonant step-up converters. The operation principle of the converter and its resonant parameter selection is presented in this paper. The operation principle of the proposed converter has been successfully verified by simulation and experimental results.**

***Index Terms*—Renewable energy, resonant converter, soft switching, voltage step-up, voltage stress.**

I. Introduction

THE development of renewable energy sources is crucial to relieve the pressures of exhaustion of the fossil fuel and environmental pollution. At present, most of the renewable energy sources are utilized with the form of ac power. The generation equipments of the renewable energy sources and energy storage devices usually contain dc conversion stages and the produced electrical energy is delivered to the power grid through dc/ac stages, resulting in additional energy loss. Moreover, the common problem of the renewable energy sources, such as wind and solar, is the large variations of output power, and the connection of large scale of the renewable sources to the power grid is a huge challenge for the traditional electrical equipment, grid structure, and operation. DC grid, as one of the solutions to the aforementioned issues, is an emerging and promising approach which has drawn much attention recently [1]–[4].

At present, the voltages over the dc stages in the generation equipments of the renewable energy sources are relatively low, in the range of several hundred volts to several thousand volts; hence, high-power high-voltage step-up dc–dc converters are required to deliver the produced electrical energy to the HVDC grid. Furthermore, as the connectors between the renewable energy sources and HVDC grid, the step-up dc–dc converters not only transmit electrical energy, but also isolate or buff kinds of fault conditions; they are one of the key equipments in the dc grid [5].

Recently, the high-power high-voltage step-up dc–dc converters have been studied extensively [5]–[29]. The transformer is a convenient approach to realize voltage step-up. The classic full-bridge (FB) converter, single active bridge (SAB) converter, and *LCC* resonant converter are studied and their performance is compared for the offshore wind farm application [7]–[10]. The three-phase topologies, such as three-phase SAB converter, series resonant converter, and dual active bridge converter, which are more suitable for high-power applications due to alleviated current stress of each bridge, are also studied and designed for high-power high-voltage step-up applications [11]–[13]. The emerging modular dc–dc converter, which uses two modular multilevel converters linked by a medium-frequency transformer, is well suited for the application in the HVDC grid [14]–[16]. For these isolated topologies, the main obstacle is the fabrication of the high-power high-voltage medium-frequency transformer and there is no report about the transformer prototype yet. Multiple small-capacity isolated converters connected in series and/or parallel to form a high-power high-voltage converter is an effective means to avoid the use of single large-capacity transformer [17]–[20].

For the application where galvanic isolation is not mandatory, the use of a transformer would only increase the cost, volume, and losses, especially for high-power high-voltage applications [21]. Several nonisolated topologies for high-power high-voltage applications have recently been proposed and studied in the literature [21]–[29]. A boost converter is adapted by the researchers of Converteam company to transmit energy from ± 50 to ± 200 kV [22]. To obtain the higher voltage gain, Enjeti *et al.* proposed a multiple-module structure, which consists of a boost converter and a buck/boost converter connected in input-parallel output-series [23]. The output power and voltage are shared by the two converters and the voltage and current ratings of switches and diodes are correspondingly reduced. However, the efficiency of a boost or buck/boost converter is relatively

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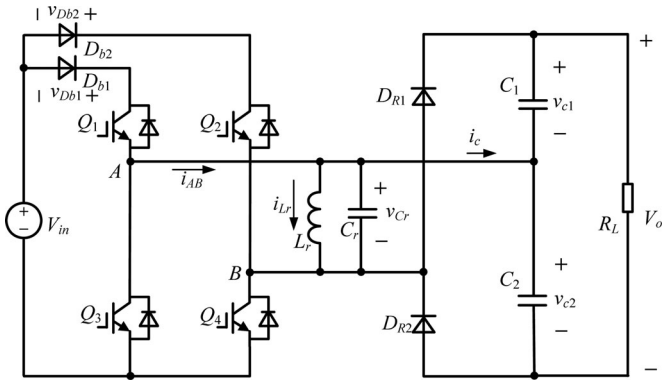

Fig. 1. Topology of the proposed resonant step-up converter.

low due to the hard switching of the active switch and the large reverse recovery loss of the diode.

The soft-switching technology is critical to improve the conversion efficiency, especially for high-voltage applications [31]–[37]. Recently, several soft-switching topologies for high-power high-voltage applications have been proposed. In [24] and [25], the converter topologies based on resonant switched capacitor (RSC) are proposed with reduced switching loss and modular structure. The shortage of the RSC-based converter is the poor voltage regulation and the requirement of a large number of capacitors. Jovcic *et al.* proposed a novel type of resonant step-up converter with potentially soft-switching operation, which utilizes thyristors as switches and does not suffer from excessive switch stresses and reverse recovery problems; moreover, a large voltage gain is easily obtained [26]–[28]. Similarly, in [29], a new family of resonant transformerless modular dc–dc converters is proposed and the main feature of the proposed converters is that the unequal voltage stress on semiconductors of thyristor valve is avoided with the use of active switching network, which is composed of an ac capacitor and four identical active switches. Thyristors have large voltage and current ratings; however, the use of thyristor limits the switching frequency of the converter, resulting in bulky passive components and slow dynamic response [30]. Moreover, the resonant inductors of the converters are unidirectional magnetized in [26]–[29], leading to lower utilization of the magnetic core, which means that a great volume of core is required.

In this paper, a novel resonant step-up dc–dc converter is proposed, which not only can realize soft switching for main switches and diodes and large voltage gain, but also has relatively lower equivalent voltage stress of the semiconductor devices and bidirectional magnetized resonant inductor. The operation principle of the converter and the design of the resonant parameters are presented in this paper. A 100 V (±20%)/1000 V, 1-kW prototype is built in the laboratory to verify the effectiveness of the converter.

II. Converter Structure and Operation Principle

The proposed resonant step-up converter is shown in Fig. 1. The converter is composed of an FB switch network, which comprises Q_1 through Q_4, an *LC* parallel resonant tank, a voltage doubler rectifier, and two input blocking diodes, D_{b1} and D_{b2}. The steady-state operating waveforms are shown in Fig. 2 and detailed operation modes of the proposed converter are shown in Fig. 3. For the proposed converter, Q_2 and Q_3 are tuned on and off simultaneously; Q_1 and Q_4 are tuned on and off simultaneously. In order to simplify the analysis of the converter, the following assumptions are made:

1) all switches, diodes, inductor, and capacitor are ideal components;
2) output filter capacitors C_1 and C_2 are equal and large enough so that the output voltage V_o is considered constant in a switching period T_s.

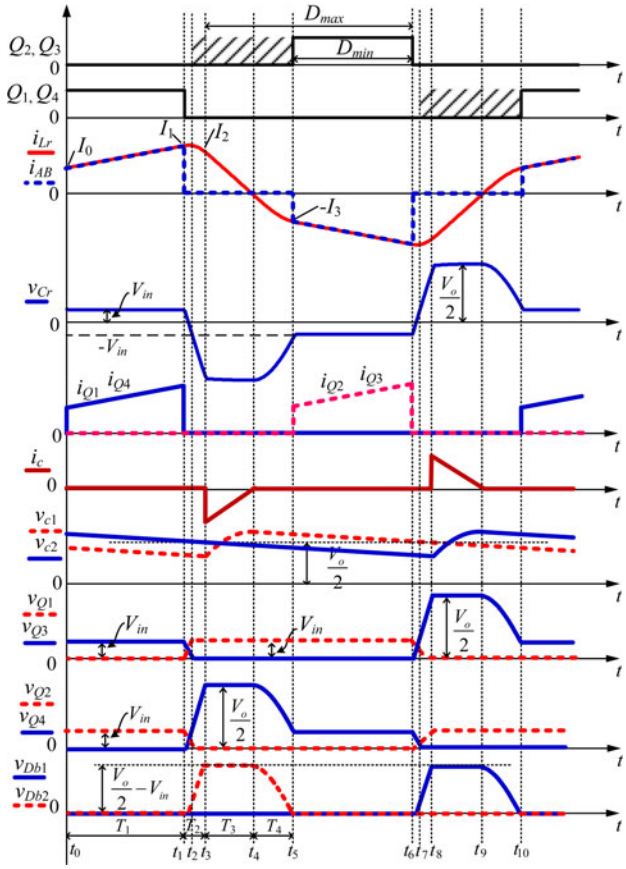

Fig. 2. Operating waveforms of the proposed converter.

A. Mode 1 [t_0, t_1] [See Fig. 3(a)]

During this mode, Q_1 and Q_4 are turned on resulting in the positive input voltage $V_{\rm in}$ across the *LC* parallel resonant tank, i.e., $v_{Lr} = v_{Cr} = V_{\rm in}$. The converter operates similar to a conventional boost converter and the resonant inductor L_r acts as the boost inductor with the current through it increasing linearly from I_0. The load is powered by C_1 and C_2. At t_1, the resonant inductor current i_{Lr} reaches I_1

$$I_1 = I_0 + \frac{V_{\rm in} T_1}{L_r} \tag{1}$$

where T_1 is the time interval of t_0 to t_1.

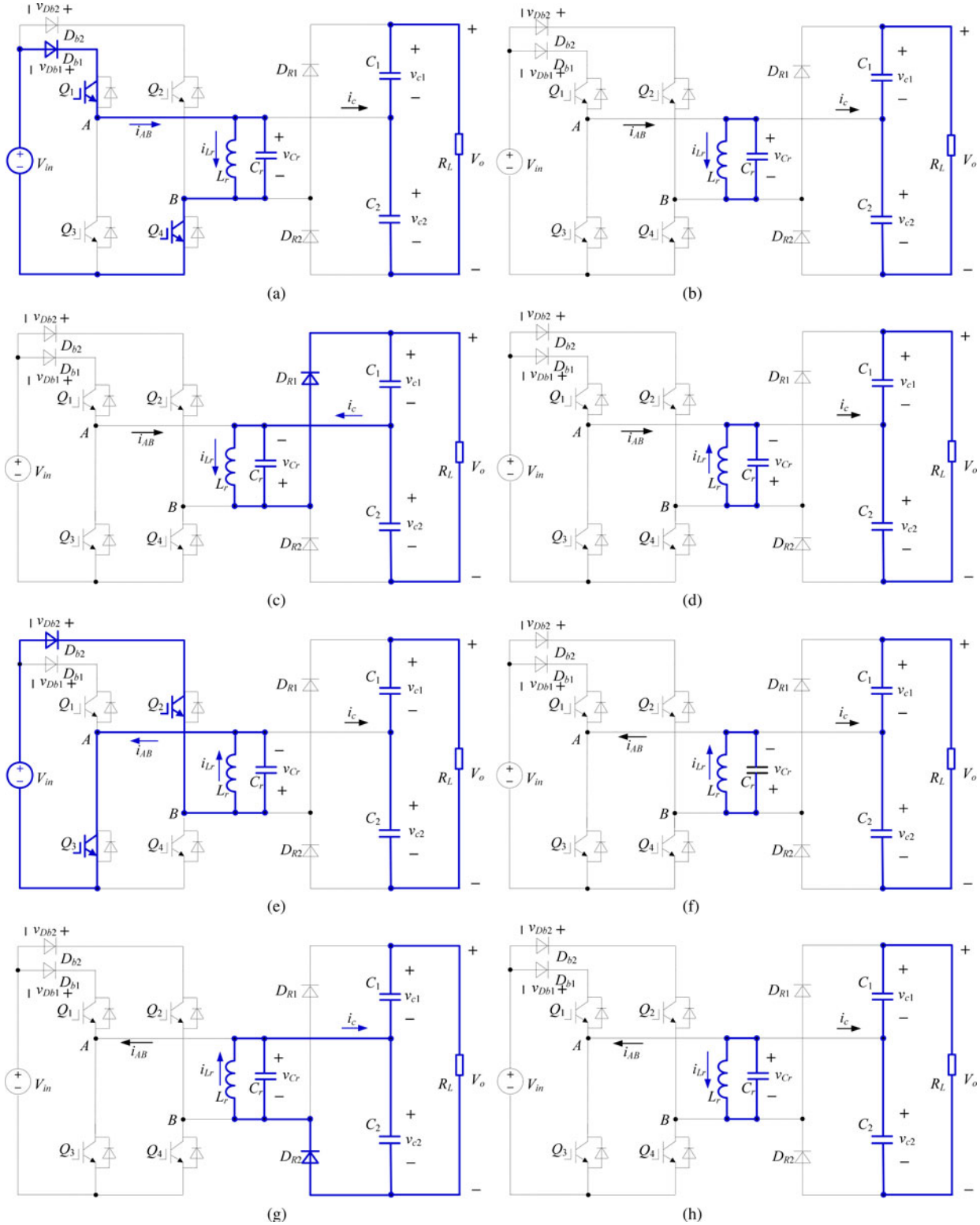

Fig. 3. Equivalent circuits of each operation stages. (a) $[t_0, t_1]$. (b) $[t_1, t_3]$. (c) $[t_3, t_4]$. (d) $[t_4, t_5]$. (e) $[t_5, t_6]$. (f) $[t_6, t_8]$. (g) $[t_8, t_9]$. (h) $[t_9, t_{10}]$.

In this mode, the energy delivered from $V_{\rm in}$ to L_r is

$$E_{\rm in} = \frac{1}{2} L_r (I_1^2 - I_0^2). \tag{2}$$

B. Mode 2 [t_1, t_3] [See Fig. 3(b)]

At t_1, Q_1 and Q_4 are turned off and after that L_r resonates with C_r, v_{Cr} decreases from $V_{\rm in}$, and i_{Lr} increases from I_1 in resonant form. Taking into account the parasitic output

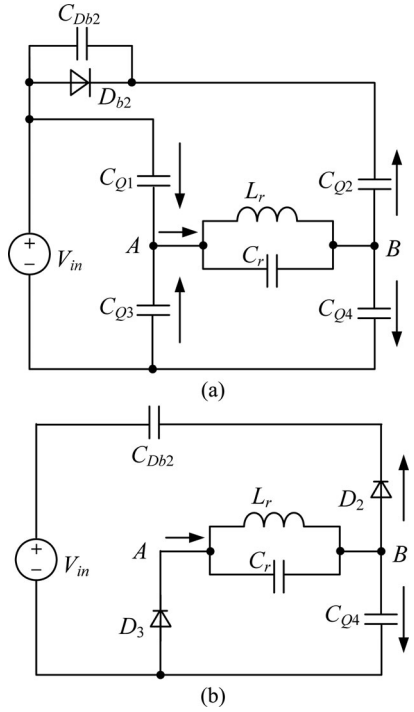

Fig. 4. Further equivalent circuits of Mode 2. (a) $[t_1, t_2]$. (b) $[t_2, t_3]$.

capacitors of Q_1 through Q_4 and junction capacitor of D_{b2}, the equivalent circuit of the converter after t_1 is shown in Fig. 4(a), in which C_{Db2}, C_{Q1}, and C_{Q4} are charged, C_{Q2} and C_{Q3} are discharged. In order to realize zero-voltage switching (ZVS) for Q_2 and Q_3, an additional capacitor, whose magnitude is about ten times with respect to C_{Q2}, is connected in parallel with D_{b2}. Hence, the voltage across D_{b2} is considered unchanged during the charging/discharging process and D_{b2} is equivalent to be shorted. Due to C_r is much larger than the parasitic capacitances, the voltages across Q_1 and Q_4 increase slowly. As a result, Q_1 and Q_4 are turned off at almost zero voltage in this mode.

When v_{Cr} drops to zero, i_{Lr} reaches its maximum magnitude. After that, v_{Cr} increases in negative direction and i_{Lr} declines in resonant form. At t_2, $v_{Cr} = -V_{\rm in}$, the voltages across Q_1 and Q_4 reach $V_{\rm in}$, the voltages across Q_2 and Q_3 fall to zero and the two switches can be turned on under zero-voltage condition. It should be noted that although Q_2 and Q_3 could be turned on after t_2, there are no currents flowing through them. After t_2, L_r continues to resonate with C_r, v_{Cr} increases in negative direction from $-V_{\rm in}$, i_{Lr} declines in resonant form. D_{b2} will hold reversed-bias voltage and the voltage across Q_4 continues to increase from $V_{\rm in}$. The voltage across Q_1 is kept at $V_{\rm in}$. The equivalent circuit of the converter after t_2 is shown in Fig. 4(b), in which D_2 and D_3 are the antiparallel diodes of Q_2 and Q_3, respectively. This mode runs until v_{Cr} increases to $-V_o/2$ and i_{Lr} reduces to I_2, at t_3, the voltage across Q_4 reaches $V_o/2$ and the voltage across D_{b2} reaches $V_o/2 - V_{\rm in}$.

It can be seen that during t_1 to t_3, no power is transferred from the input source or to the load, and the whole energy stored in the *LC* resonant tank is unchanged, i.e.,

$$\frac{1}{2}L_r I_1^2 + \frac{1}{2}C_r V_{\rm in}^2 = \frac{1}{2}L_r I_2^2 + \frac{1}{2}C_r \left(\frac{V_o}{2}\right)^2. \tag{3}$$

We have

$$i_{Lr}(t) = \frac{V_{\rm in}}{\rm Z_r}\sin\left[\omega_r(t-t_1)\right] + I_1\cos\left[\omega_r(t-t_1)\right] \tag{4}$$

$$v_{Cr}(t) = V_{\rm in}\cos\left[\omega_r(t-t_1)\right] - I_1 {\rm Z}_r \sin\left[\omega_r(t-t_1)\right] \tag{5}$$

$$T_2 = \frac{1}{\omega_r}\left[\arcsin\left(\frac{V_{\rm in}}{\sqrt{V_{\rm in}^2 + \frac{L_r I_1^2}{C_r}}}\right) + \arcsin\left(\frac{V_o}{2\sqrt{V_{\rm in}^2 + \frac{L_r I_1^2}{C_r}}}\right)\right] \tag{6}$$

where $\omega_r = 1/\sqrt{L_r C_r}$, $Z_r = \sqrt{L_r/C_r}$, and T_2 is the time interval of t_1 to t_3.

C. Mode 3 [t_3, t_4] [See Fig. 3(c)]

At t_3, $v_{Cr} = -V_o/2$, D_{R1} conducts naturally, C_1 is charged by i_{Lr} through D_{R1}, v_{Cr} keeps unchanged, and i_{Lr} decreases linearly. At t_4, $i_{Lr} = 0$. The time interval of t_3 to t_4 is

$$T_3 = \frac{2I_2 L_r}{V_o}. \tag{7}$$

The energy delivered to load side in this mode is

$$E_{\rm out} = \frac{V_o I_2 T_3}{4}. \tag{8}$$

The energy consumed by the load in half-switching period is

$$E_R = \frac{V_o I_o T_s}{2}. \tag{9}$$

Assuming 100% conversion efficiency of the converter and according to the energy conversation rule, in half-switching period

$$E_{\rm in} = E_{\rm out} = E_{\rm R}. \tag{10}$$

Combining (7), (8), (9), and (10), we have

$$I_2 = V_o\sqrt{\frac{I_o T_s}{V_o L_r}} \tag{11}$$

$$T_3 = 2\sqrt{\frac{T_s I_o L_r}{V_o}}. \tag{12}$$

D. Mode 4 [t_4, t_5] [See Fig. 3(d)]

At t_4, i_{Lr} decreases to zero and the current flowing through D_{R1} also decreases to zero, and D_{R1} is turned off with zero-current switching (ZCS); therefore, there is no reverse recovery. After t_4, L_r resonates with C_r, C_r is discharged through L_r, v_{Cr} increases from $-V_o/2$ in positive direction, and i_{Lr} increases from zero in negative direction. Meanwhile, the voltage across Q_4 declines from $V_o/2$. At t_5, $v_{Cr} = -V_{\rm in}$, and $i_{Lr} = -I_3$. In

TABLE I
COMPARISON OF DIFFERENT NONISOLATED CONVERTER TOPOLOGIES

Topologies	Voltage stress	Soft switching	Voltage regulation	Switching frequency	Output fault shorts input	Input fault shorts output
Refs.[22], [23]	Low	No	Good	Constant	Yes	No
Refs.[24], [25]	Low	Yes	Poor	Constant	Yes	Yes
Refs.[26]–[28]	High	Yes	Good	Variable	No	No
Ref.[29]	High	Yes	Good	Variable	Yes	No
Proposed one	Medium	Yes	Good	Variable	No	No

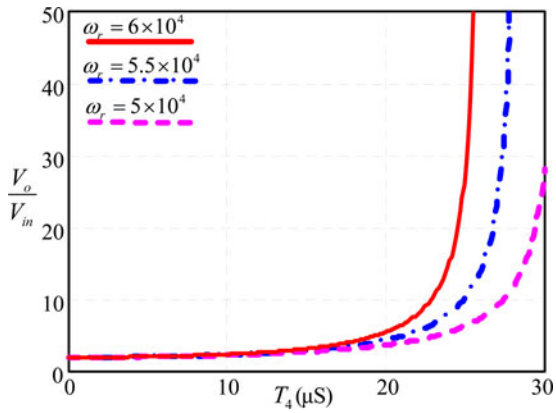

Fig. 5. Voltage gain versus ω_r and T_4.

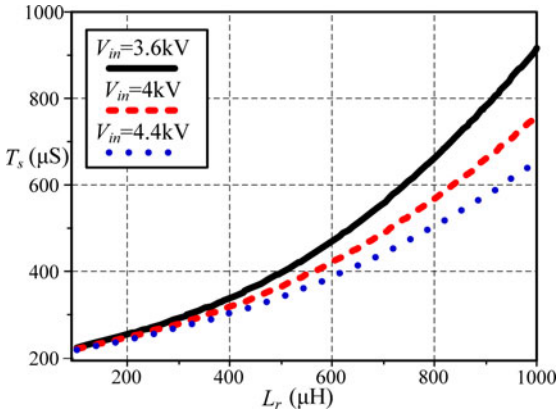

Fig. 6. Curves between L_r and T_s under different input voltages.

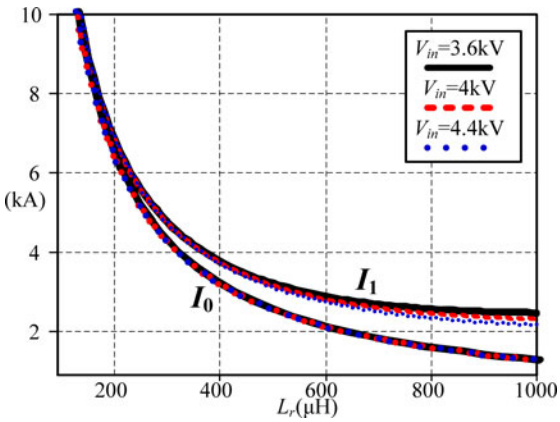

Fig. 7. Curves between L_r and I_0, I_1 under different input voltages.

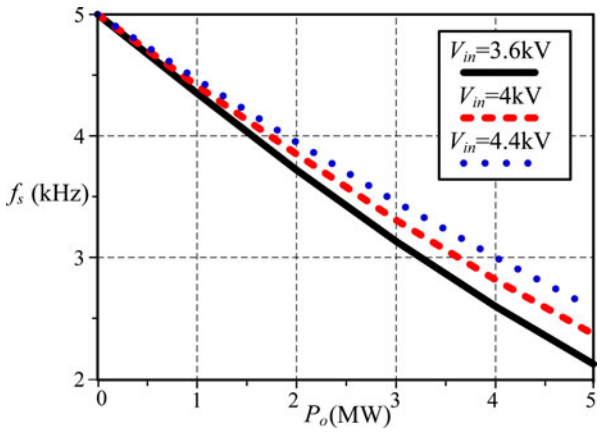

Fig. 8. Curves of switching frequency versus output power under different input voltages.

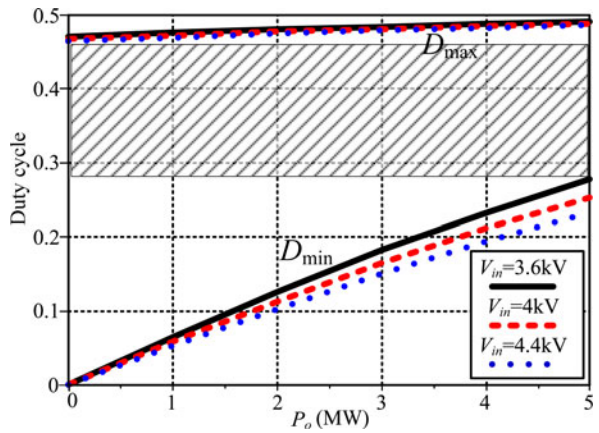

Fig. 9. Curves of $D_{\min}$ and $D_{\max}$ versus output power under different input voltages.

TABLE II
SIMULATION PARAMETERS

Item	Symbol	Value
Input voltage	V_{in}	3.6–4.4 kV
Output voltage	V_o	80 kV
Resonant inductance	L_r	600 μH
Resonant capacitance	C_r	1.68 μF
Filter capacitance	C_1, C_2	22 μF
Duty cycle	D	0.4

this mode, the whole energy stored in the *LC* resonant tank is unchanged, i.e.,

$$\frac{1}{2}C_r\left(\frac{V_o}{2}\right)^2 = \frac{1}{2}L_r I_3^2 + \frac{1}{2}C_r V_{\text{in}}^2. \tag{13}$$

We have

$$I_0 = I_3 = \frac{1}{2}\sqrt{\frac{C_r(V_o^2 - 4V_{\text{in}}^2)}{L_r}} \tag{14}$$

$$i_{Lr}(t) = -\frac{V_o}{2\omega_r L_r}\sin\left[\omega_r(t - t_5)\right] \tag{15}$$

$$v_{Cr}(t) = \frac{-V_o\cos\left[\omega_r(t - t_5)\right]}{2} \tag{16}$$

$$T_4 = \frac{1}{\omega_r}\arccos\left(\frac{2V_{\text{in}}}{V_o}\right) \tag{17}$$

where T_4 is the time interval of t_4 to t_5.

E. Mode 5 [t_5, t_6] [See Fig. 3(e)]

If Q_2 and Q_3 are turned on before t_5, then after t_5, L_r is charged by V_{in} through Q_2 and Q_3, i_{Lr} increases in negative direction, and the mode is similar to Mode 1.

If Q_2 and Q_3 are not turned on before t_5, then after t_5, L_r will resonate with C_r, the voltage of node *A* v_A will increase from zero and the voltage of node *B* v_B will decay from V_{in}; zero-voltage condition will be lost if Q_2 and Q_3 are turned on at the moment. Therefore, Q_2 and Q_3 must be turned on before t_5 to reduce switching loss.

The operation modes during [t_6, t_{10}] are similar to Modes 2–4, and the detailed equivalent circuits are shown in Fig. 3(f)–(h). During [t_6, t_{10}], Q_2 and Q_3 are turned off at almost zero voltage, Q_1 and Q_4 are turned on with ZVS, and D_{R2} is turned off with ZCS.

III. Analysis and Design of the Converter

A. Voltage Rating and DC Fault Response

According to the analysis of Section II, the voltage stresses of Q_1 and Q_2 are the input voltage V_{in}, the voltage stresses of Q_3 and Q_4 are half of the output voltage, i.e., $V_o/2$, the voltage stresses of D_{b1} and D_{b2} are $V_o/2 - V_{\text{in}}$. The total voltage stress of the primary semiconductor devices is $2V_o$, which is half of that in [26]–[29]. It implies that much less semiconductor devices are required in the proposed step-up converter, resulting in low conduction and switching losses and low cost. Moreover, the peak voltages across the resonant inductor and resonant capacitor are $V_o/2$, which is also half of that in [26]–[29]. Lower peak voltage indicates that the insulation is easy to be implemented, leading to the reduction of the size of the resonant tank.

As shown in Fig. 1, the proposed converter can block an output fault and prevent the fault pass through input side, and vice versa. The comparison of different nonisolated converter topologies is listed in Table I.

B. Voltage Balance Between C_1 and C_2

The previous analysis is based on the assumption that voltages across C_1 and C_2 are, respectively, half of output voltage. Provided that $V_{c1} \neq V_{c2}$, for example, $V_{c1} > V_o/2 > V_{c2}$, according to the operation principle of Fig. 2, the peak current of i_c at t_3 will be smaller than that at t_8, which means that the average current flowing into C_1 will be smaller than the average current flowing into C_2. Due to C_1 and C_2 power the same load, therefore, V_{c1} decreases and V_{c2} increases, and finally they share the same output voltage. Vice versa, i.e., V_{c1} increases and V_{c2} decreases under the presumption that $V_{c1} < V_o/2 < V_{c2}$.

C. Analysis of the Converter

From Fig. 2, we have

$$T_1 + T_2 + T_3 + T_4 = \frac{T_s}{2}. \tag{18}$$

Combining (1), (2), and (14) yields

$$V_o I_o T_s = \frac{V_{\text{in}}^2 T_1^2}{L_r} + V_{\text{in}} T_1\sqrt{\frac{C_r(V_o^2 - 4V_{\text{in}}^2)}{L_r}}. \tag{19}$$

From (19), we have

$$T_1 = \frac{\sqrt{\frac{C_r(V_o^2 - 4V_{\text{in}}^2) + 4V_o I_o T_s}{L_r}} - \sqrt{\frac{C_r(V_o^2 - 4V_{\text{in}}^2)}{L_r}}}{2\frac{V_{\text{in}}}{L_r}}. \tag{20}$$

From (17), the gain of V_o/V_{in} is expressed as

$$\frac{V_o}{V_{\text{in}}} = \frac{2}{\cos(\omega_r T_4)}. \tag{21}$$

It can be seen that the gain of V_o/V_{in} is impacted by the parameters of the resonant tank (L_r and C_r) and the time interval of t_4 to t_5, which is a part of switching period; hence, in other words, the gain is impacted by L_r, C_r, and the switching frequency. Several important conclusions are obtained from (21).

1) For any given voltage gain (larger than 2) and the resonant tank parameters L_r and C_r, there must be a T_4 to meet (21), which implies that for given L_r and C_r, the voltage gain can be infinite if the switching frequency range is not taken into account.
2) For given voltage gain, the larger the ω_r, the shorter the T_4; an example is shown in Fig. 5, which means that the switching frequency will be higher.
3) For given voltage gain and ω_r, although T_4 is constant, but the expressions of T_1, T_2, and T_3 are related to L_r or C_r, which means that different pairs of L_r and C_r impact the switching frequency of the proposed converter.

Substituting (20) into (1) yields

$$I_1 = \sqrt{\frac{C_r(V_o^2 - 4V_{\text{in}}^2) + 4V_o I_o T_s}{4L_r}}. \tag{22}$$

Substituting (22) into (3) yields

$$I_2 = \sqrt{\frac{V_o I_o T_s}{L_r}}. \tag{23}$$

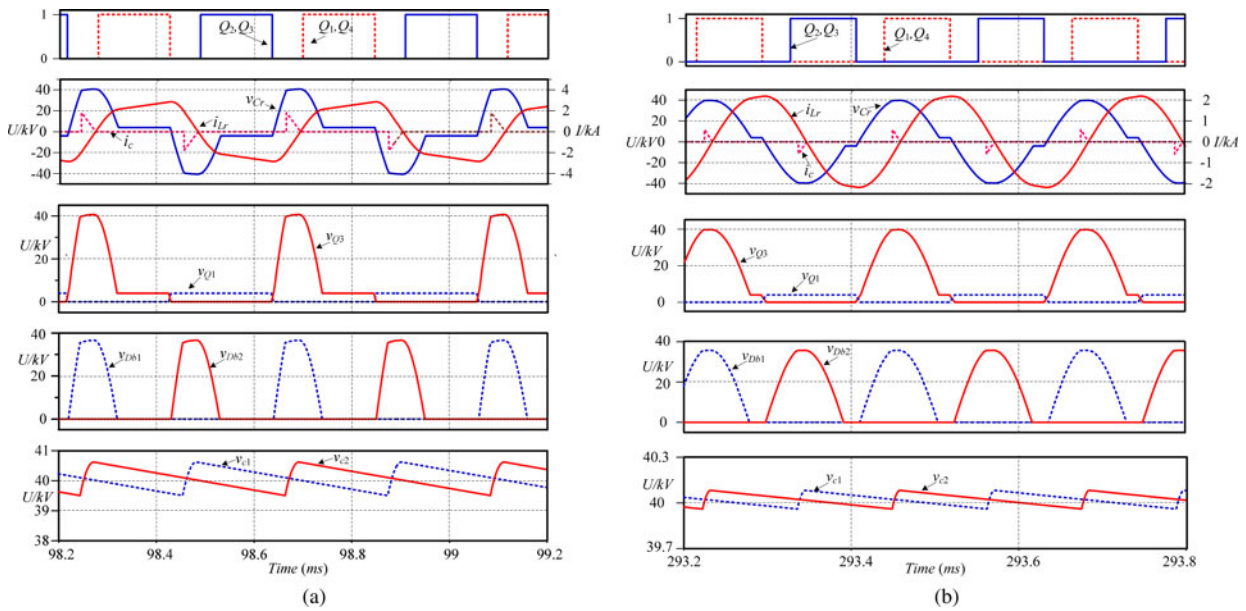

Fig. 10. Steady-state simulation results under different load conditions when $V_{\rm in} = 4$ kV. (a) 5 MW. (b) 1 MW.

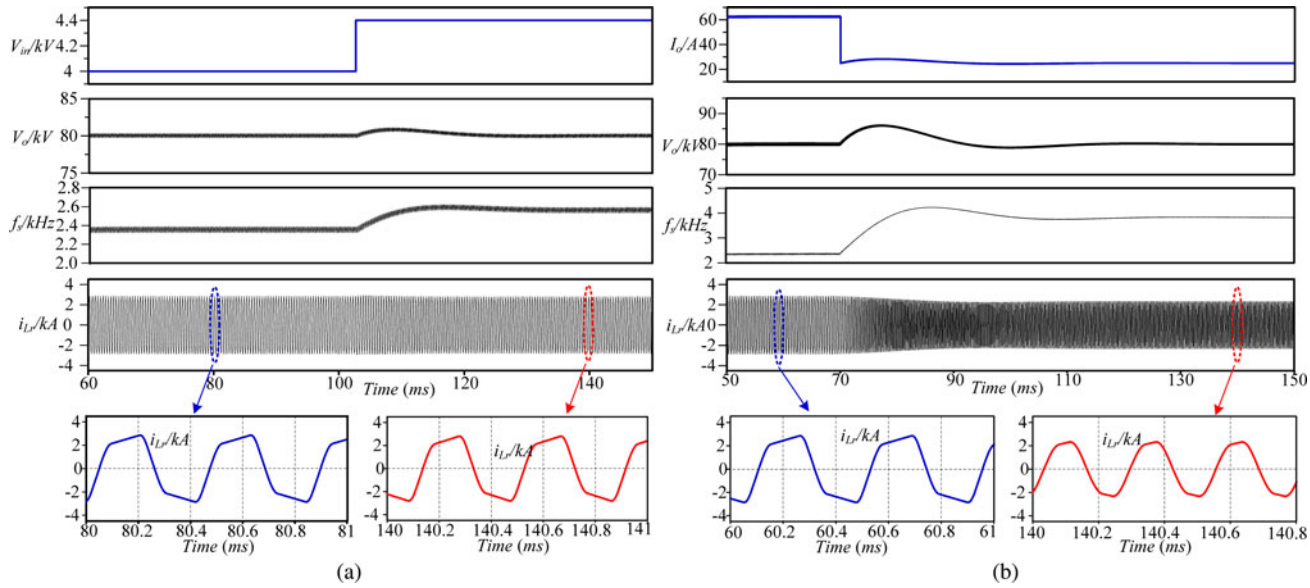

Fig. 11. Dynamic simulation results. (a) Input voltage step. (b) Load step.

Substituting (22) into (6) yields

$$T_2 = \frac{1}{\omega_r}\left[\arcsin\left(\frac{2V_{\rm in}}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right) + \arcsin\left(\frac{V_o}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right)\right] \tag{24}$$

Combining (12), (17), (18), (20), and (24), we have

$$+\frac{1}{\omega_r}\left[\arcsin\left(\frac{2V_{\rm in}}{\sqrt{V_o^2+\frac{4V_o I_o T_s}{C_r}}}\right) + \arcsin\left(\frac{V_o}{\sqrt{V_o^2+\frac{4V_o I_o T_s}{C_r}}}\right)\right]$$
$$+2\sqrt{\frac{T_s I_o L_r}{V_o}} + \frac{1}{\omega_r}\arccos\left(\frac{2V_{\rm in}}{V_o}\right) = \frac{T_s}{2}. \tag{25}$$

From (25), we can obtain the following equation under unloaded condition ($I_o = 0$):

$$f_s = f_r(I_o = 0) \tag{26}$$

$$\frac{\sqrt{\frac{C_r(V_o^2 - 4V_{\rm in}^2) + 4V_o I_o T_s}{L_r}} - \sqrt{\frac{C_r(V_o^2 - 4V_{\rm in}^2)}{L_r}}}{2\frac{V_{\rm in}}{L_r}}$$

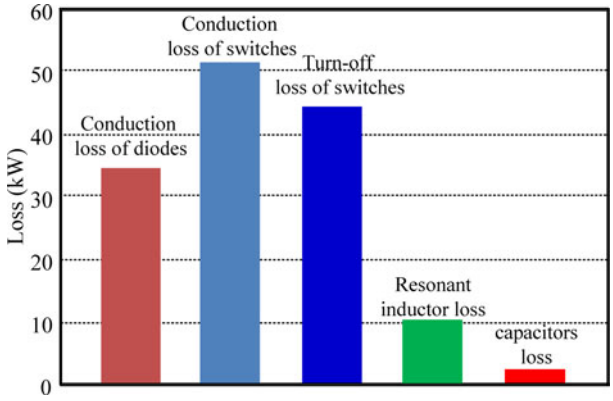

Fig. 12. Calculated power losses distribution.

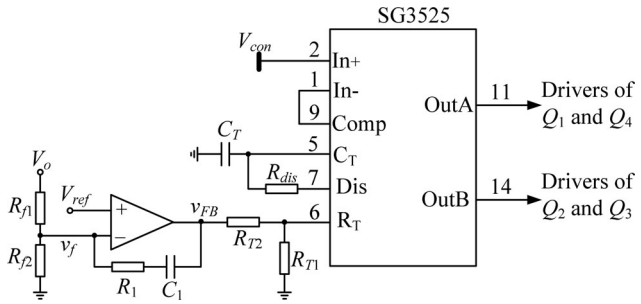

Fig. 13. Block diagram of the control circuit.

where f_s is the switching frequency and f_r is the resonant frequency of L_r and C_r, i.e.,

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{27}$$

It can be seen that the switching frequency is equal to the resonant frequency under unloaded condition. Actually, it can be seen from Fig. 2 that $T_1 = T_3 = 0$ under unloaded condition because there is no energy input and output if the converter is assumed to be lossless. And if $I_o > 0$, then both T_1 and T_3 are larger than zero; thus, the switching frequency is lower than the resonant frequency; the heavier the load, the lower the switching frequency. Therefore, the maximum switching frequency of the converter is

$$f_{s\max} = f_r. \tag{28}$$

From the analysis of Section II, it can be seen that to realize zero-voltage turn-on of the switches, the minimum duty cycle of the converter is

$$D_{\min} = T_1/T_s. \tag{29}$$

As shown in Fig. 2 and the previous analysis, the minimum duty cycle also is the effective duty cycle of the converter, during which the primary current flows through the main switches.

According to (5), the time interval ΔT of t_1 to t_2 is

$$\Delta T = \frac{2}{\omega_r}\arcsin\left(\frac{2V_{\text{in}}}{\sqrt{V_o^2 + \frac{4V_o I_o T_s}{C_r}}}\right). \tag{30}$$

The maximum duty cycle of the converter is

$$D_{\max} = \frac{T_s/2 - \Delta T}{T_s}. \tag{31}$$

D. Design of the Converter

A 5 MW, 4 kV (±10%)/80 kV step-up converter is taken as an example to design the parameters. Insulated-gate bipolar transistors (IGBTs) are taken as the main switches and $f_{s\max}$ is set to be 5 kHz.

From (25), one can obtain the expression of T_s associated with L_r under full-load condition. However, (25) indicates that T_s is an implicit function associated with L_r and the concrete analytic solution of T_s cannot be obtained. With the help of mathematical analysis software Maple, we can obtain the curves between L_r and T_s under different input voltages as shown in Fig. 6. It can be seen that for given V_o and L_r, the lower the input voltage V_{in}, the lower the switching frequency, and for given input voltage range, the smaller the L_r, the narrower the variation of switching frequency.

From (14), one can obtain the curves between L_r and I_0 under different input voltages, as shown in Fig. 7. Through (22) and (25), one can obtain the curves between L_r and I_1 under different input voltages, as shown in Fig. 7. It can be seen that the input voltage has little influence on I_0 and I_1, because as shown in (14) and (22), the larger the voltage gain, the lesser the influence of the input voltage on I_0 and I_1.

From Fig. 6, it can be seen that the smaller the L_r, the shorter the T_s under full-load condition, which means that the converter has relatively narrower range of switching frequency because the maximum switching frequency is fixed, and it is beneficial to the design of input/output filters and resonant inductor. On the contrary, the larger the L_r, the longer the T_s under full-load condition, which means that the converter has relatively wider range of switching frequency and it is disadvantageous to the design of input/output filters and resonant inductor. From Fig. 7, it can be seen that the smaller the L_r, the larger the I_0 and I_1, which means that switches and diodes have large peak currents and it is harmful for the device choice, while larger L_r is helpful for the device choice. Hence, there is a tradeoff when designing the resonant parameters. The final selection of L_r is 600 μH, C_r is 1.68 μF, and the minimum switching frequency is 2.1 kHz, and the peak current of the semiconductor devices is 2850 A, which is about two times of the average input current.

After the choice of the resonant parameters, the relationship between the switching frequency and power load is depicted in Fig. 8 with (25). As the figure shows, the range of the switching frequency is 2.1–5 kHz in the whole load and input voltage range. The switching frequency depends on the output power and the switching frequency drops almost linearly with the increasing of the output power. According to (29) and (31), the curves of $D_{\min}$ and $D_{\max}$ with respect to output power under different input voltages are shown in Fig. 9. As the figure shows, both $D_{\min}$ and $D_{\max}$ depend on the output power, the maximum of $D_{\min}$ is 0.277, and the minimum of $D_{\max}$ is 0.465. Thus, to realized ZVS for the switches, the duty cycle

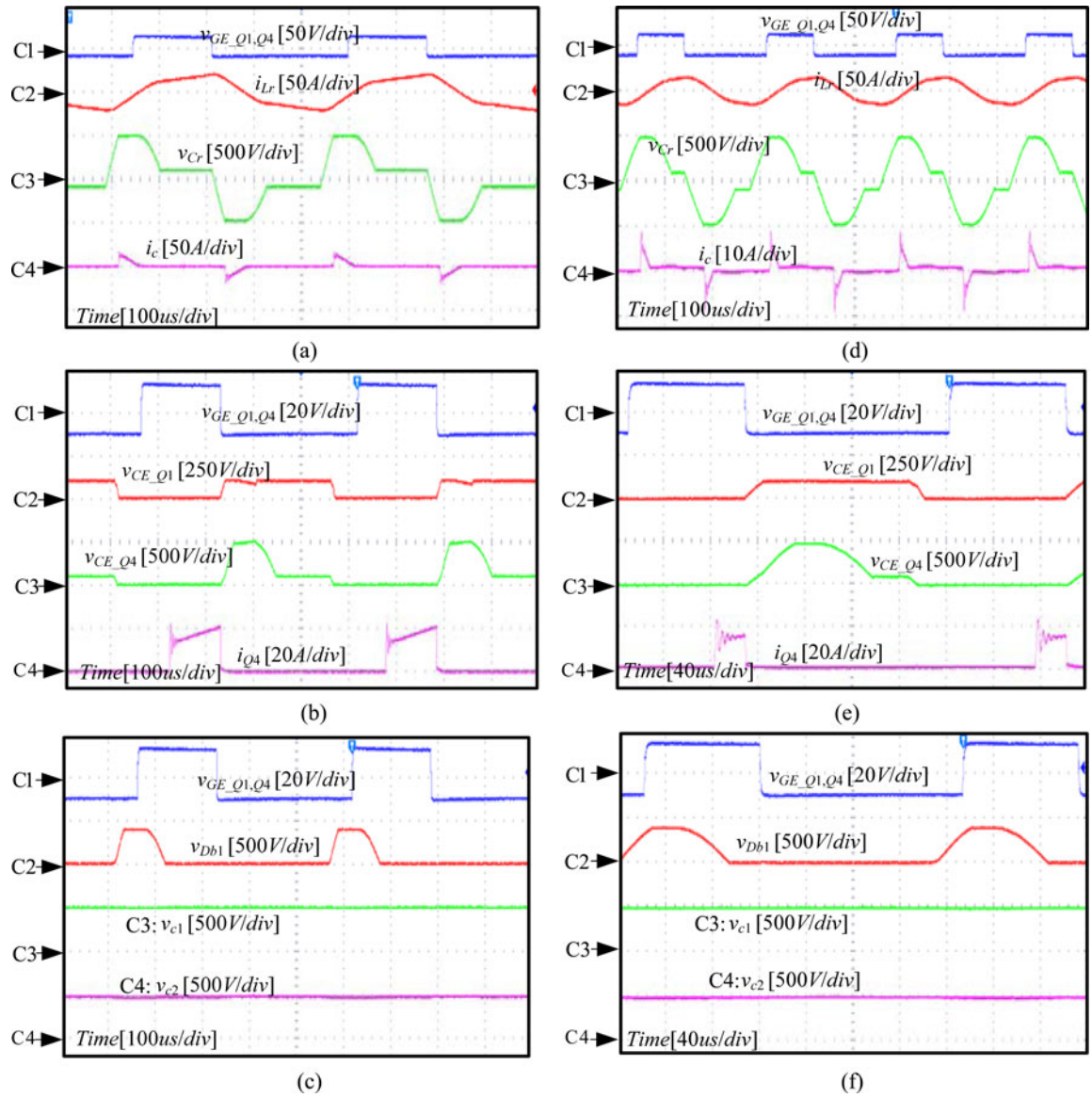

Fig. 14. Experimental waveforms under (a)–(c) 1 kW and (d)–(f) 200 W load conditions when $V_{\rm in} = 100$ V. (a), (d) v_{GE} of Q_1, current of L_r, voltage across C_r and i_c. (b), (e) v_{GE} of Q_1, v_{CE} of Q_1, v_{CE} of Q_4, and current of Q_4. (c), (f) v_{GE} of Q_1, voltage across D_{b1}, and voltages across C_1 and C_2.

can be the any value in the range of 0.277–0.465, as the shaded area shown in Fig. 9. Therefore, the control of the proposed converter is very simple with constant duty cycle and variable switching frequency.

IV. Simulation and Experimental Results

In order to verify the operation principle and the theoretical analysis, a converter is simulated with PLECS simulation software and the detailed parameters are listed in Table II. All switches used in PLECS simulation are ideal switches and 5 nF capacitance is added in parallel with D_{b1} and D_{b2}.

Fig. 10 shows the simulation results at the output power of 5 and 1 MW ($V_{\rm in} = 4$ kV), respectively. As the figure shows, the voltage stress of Q_1 and Q_2 is 4 kV, the voltage stress of Q_3 and Q_4 is 40 kV, the voltage stress of D_{b1} and D_{b2} is 36 kV, and the peak voltage across the *LC* resonant tank is 40 kV. Q_1 through Q_4 are turned on under zero-voltage condition and when they are turned off, the voltage across the device increases slowly from zero. The switching frequencies of the converter at 5 and 1 MW are 2.3 and 4.4 kHz, respectively. The simulation results match well with the aforementioned analysis.

Fig. 11(a) illustrates the simulation results corresponding to a step change of input voltage from 4 to 4.4 kV under full-load condition. It can be seen that the output voltage is regulated to be constant and the switching frequency f_s changes from 2.3 to 2.5 kHz. Fig. 11(b) illustrates the simulation results corresponding to a load stepping from full load to 40% load under 4 kV input voltage condition. It can be seen that the output voltage is regulated to be constant and the switching frequency f_s changes from 2.3 to 3.8 kHz. The simulation results match well with Fig. 8 and the control strategy of variable frequency with constant duty cycle is validated.

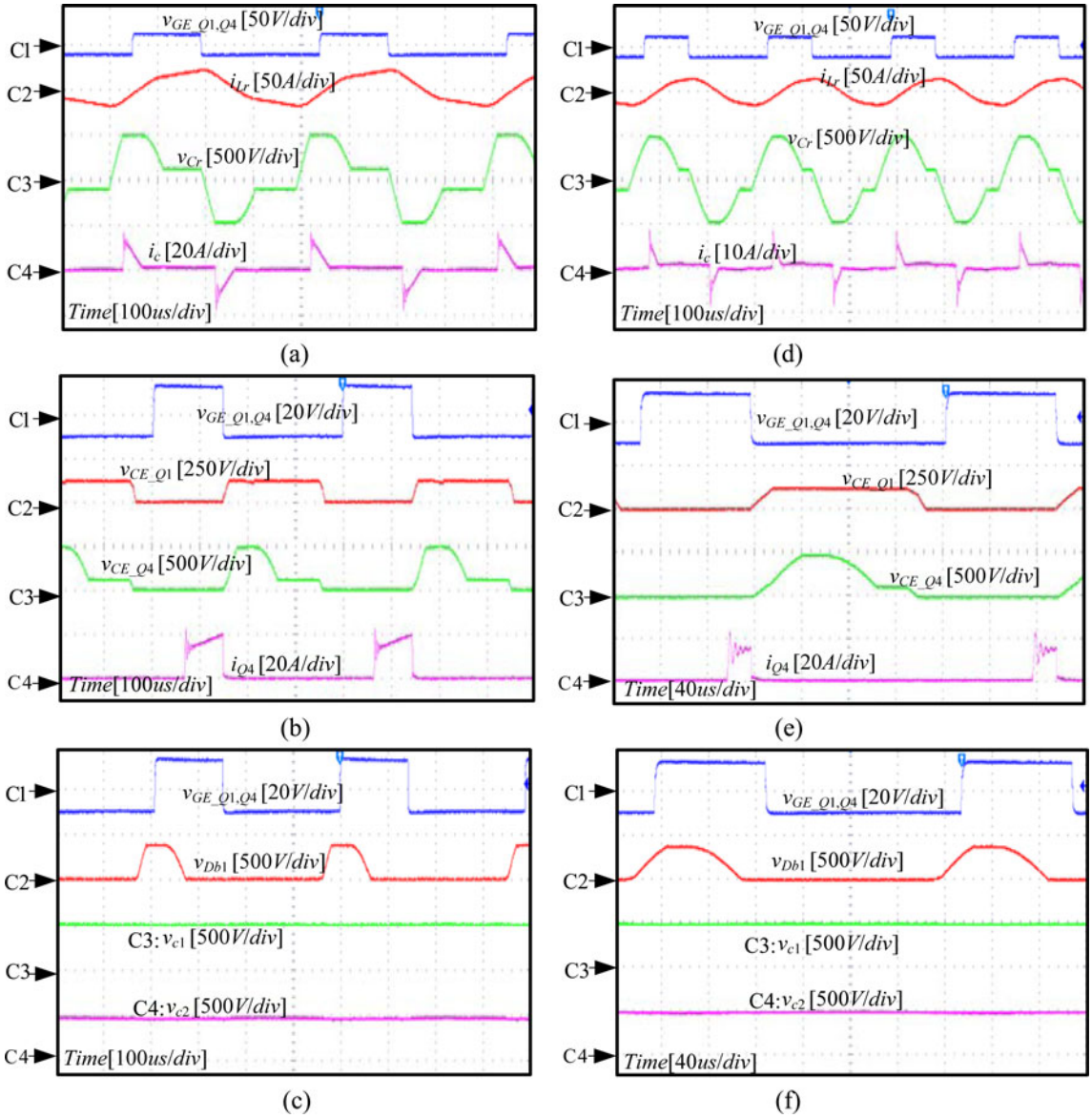

Fig. 15. Experimental waveforms under (a)–(c) 1 kW and (d)–(f) 200 W load conditions when $V_{\rm in} = 120$ V. (a), (d) v_{GE} of Q_1, current of L_r, voltage across C_r and i_c. (b), (e) v_{GE} of Q_1, v_{CE} of Q_1, v_{CE} of Q_4, and current of Q_4. (c), (f) v_{GE} of Q_1, voltage across D_{b1}, and voltages across C_1 and C_2.

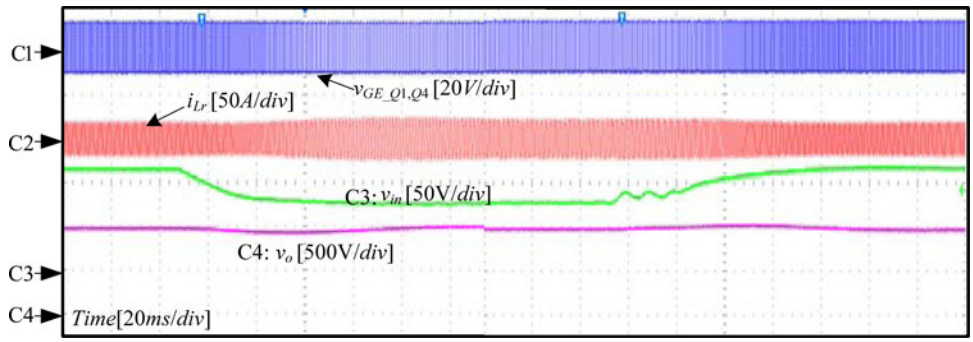

Fig. 16. Experimental waveforms of an input voltage step change.

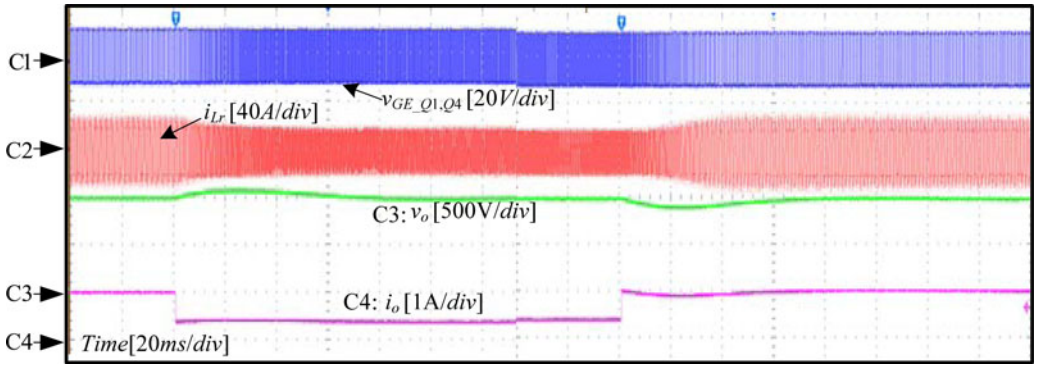

Fig. 17. Experimental waveforms of a load step change.

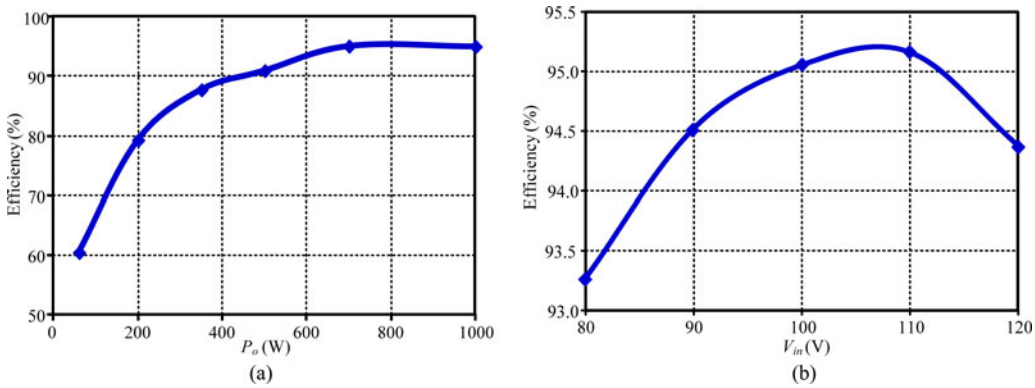

Fig. 18. Conversion efficiency of the proposed converter. (a) Efficiency at different output power under normal input voltage. (b) Efficiency at full load under different input voltages.

The efficiency and losses distribution of the 5 MW condition is also calculated. HiPak IGBT module 5SNA 0600G650100 (6500 V, 600 A) from ABB is used as the active switches. In the calculation, ten 6500 V IGBTs are connected in series to hold up 40 kV. HiPak diode module 5SLD 0600J650100 (6500 V, 1200 A) from ABB is used as the input blocking diodes and rectifier diodes. The core material of the resonant inductor is VITROPERM 500 F. Suitable high-voltage capacitors are chosen from EACO. The calculated efficiency is around 97.2% and the losses distribution is depicted in Fig. 12. It can be observed that the dominant part of the power losses is the conduction loss of diodes and switches. Although the turn-on loss is eliminated due to zero-voltage turn-on condition, because of the tail current characteristic, the turn-off loss of the IGBTs can only be alleviated thanks to the slow increasing of the voltage across the active switch. If the high-voltage large-current silicon carbide (SiC) MOSFET is available in the future [24], the turn-off loss of the converter could be reduced significantly.

In order to verify the operation of the proposed converter, a 100 V ($\pm$20%)/1000 V, 1 kW prototype converter was built in our laboratory. The parameters are $L_r = 1200$ μH, $C_r = 0.8$ μF, $C_1 = C_2 = 150$ μF, $Q_1 - Q_4$ are FF200R17KE3, the antiparallel diodes of other FF200R17KE3 are taken as the D_{b1} and D_{b2}, and rectifier diode is DSDI60-18A.

The main control block of the proposed converter is shown in Fig. 13. The conventional pulse width modulation control IC SG3525 is used with variable frequency operation. A constant voltage is connected to Pin 2 to determine a constant duty cycle. The oscillator frequency of the SG3525 is determined by the R_T and C_T, which are connected to Pin 6 and Pin 5, respectively. Hence, by connecting an external resistor (R_{T2}) to Pin 6 with a variable voltage (v_{FB}), a voltage controlled oscillator is obtained and the variable frequency constant duty cycle modulation is realized. According to Fig. 8, the output power of the converter is decreased with the increase of the switching frequency. Hence, the stable output voltage regulation process of the variable frequency controller can be expressed as $V_o \uparrow \rightarrow v_f \uparrow \rightarrow v_{FB} \downarrow \rightarrow f_s \uparrow \rightarrow P_o \downarrow \rightarrow V_o \downarrow \rightarrow V_o$ constant.

Fig. 14 shows the experimental waveforms of the converter under 1 kW and 200 W conditions with 100 V input voltage, respectively. Fig. 15 shows the experimental waveforms of the converter under 1 kW and 200 W conditions with 120 V input voltage, respectively. As Fig. 14 shows, the voltage stress of Q_1 is 100 V, the voltage stress of Q_4 is 500 V, the voltage stress of D_{b1} is 400 V, and the peak voltage across the *LC* resonant tank is 500 V. The collector–emitter voltages v_{CE_Q1} and v_{CE_Q4} have been zero when Q_1 and Q_4 are turned on; hence, they are turned on with zero voltage. The increase of v_{CE_Q4} is slow when Q_4 is turned off; hence, it is turned off with almost zero voltage. The oscillation of i_{Q4} is caused by the parasitic inductor of the prototype. All the waveforms agree well with the expected switching sequence in Fig. 2.

Fig. 16 illustrates the output voltage corresponding to a step change of input voltage varying between 80 and 120 V. Fig. 17 illustrates the output voltage corresponding to a step change of load current varying between 1 and 0.4 A. As seen, the output voltage can be regulated to be constant corresponding to the input voltage step change and load step change.

Fig. 18 shows the conversion efficiency of the proposed converter. Fig. 18(a) shows the efficiency at different output currents under normal input voltage of 100 V. Fig. 18(b) shows the efficiency at full load under different input voltages. It is shown that the maximum efficiency can be up to 95.2%.

As Fig. 18(a) shows, the efficiency decreases with the decrease of the output power, because the switching frequency is higher at light load than that at heavy load (see Fig. 8), so the turn-off loss of switches increases at light load and is the main part of the loss.

For the constant output power, the average input current decreases with the increase of the input voltage; hence, the conduction loss will decrease with the increase of the input voltage. However, the switching frequency increases with the increase of the input voltage (see Fig. 8); hence, the switching loss (turn-off loss) will increase with the increase of the input voltage. So, there is an optimum efficiency working point in the input voltage range, as shown in Fig. 18(b).

V. Conclusion

A novel resonant dc–dc converter is proposed in this paper, which can achieve very high step-up voltage gain and it is suitable for high-power high-voltage applications. The converter utilizes the resonant inductor to deliver power by charging from the input and discharging at the output. The resonant capacitor is employed to achieve zero-voltage turn-on and turn-off for the active switches and ZCS for the rectifier diodes. The analysis demonstrates that the converter can operate at any gain value (> 2) with proper control; however, the parameters of the resonant tank determine the maximum switching frequency, the range of switching frequency, and current ratings of active switches and diodes. The converter is controlled by the variable switching frequency. Simulation and experimental results verify the operation principle of the converter and parameters selection of the resonant tank.

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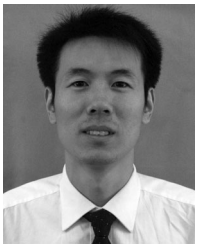

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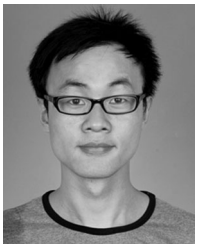

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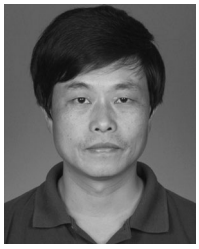

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